IN THE CLAIMS

1. (Previously Presented) A device to control a sense amplifier, comprising:

a resetable control circuit containing a first input, a second input, a third input, and an output; said first input coupled to said output or to a ground; said second input coupled to receive a start signal; said third input coupled to receive output signals of said sense amplifier; and said output coupled to said sense amplifier;

a reset signal generator, containing a first input coupled to an OUT end of said sense amplifier, a second input coupled to an OUTB end of said sense amplifier, and an output coupled to said third input of said resetable control circuit; and when either OUT or OUTB reaches a predetermined low voltage level, said output of said reset signal generator goes high.

2. (Cancelled)

3. (Cancelled)

4. (Original) The device of claim 1 wherein said resetable control circuit is a flip-flop circuit.

5. (Original) The device of claim 4 wherein said flip-flop circuit is a D flip-flop circuit.

6. (Original) The device of claim 5 wherein said first input is a data signal for said D flip-flop circuit.

7. (Original) The device of claim 5 wherein said start signal is a triggered clock for said D flip-flop circuit.

8. (Original) The device of claim 7 wherein said start signal is a pseudo word line signal.

9. (Original) The device of claim 5 wherein said third input is a reset signal for said D flip-flop circuit.

10. (Cancelled.)

11. (Original) The device of claim 5 wherein said resetable control circuit further comprises a first passgate, a second passgate, a third passgate, and fourth passgate; a first inverter, a second inverter, a third inverter, a fourth inverter, a fifth inverter, and a sixth inverter; and a first NAND gate;

said first input of said resetable control circuit coupled to an input end of said first passgate, an output end of said first passgate coupled to an output end of said second passgate and an input end of said third inverter;

said second input of said resetable control circuit coupled to an input end of said first inverter; a C end of said first passgate, a CB end of said second passgate, a CB end of said third passgate, and a C end of said fourth passgate;

said third input of said resetable control circuit coupled to an input end of said second inverter;

an output end of said first inverter coupled to a CB end of said first passgate, a C end of said second passgate, a C end of said third passgate, and a CB end of said fourth passgate;

an output end of said third inverter coupled to a first input end of said first NAND gate and to an input end of said third passgate;

an output end of said second inverter coupled to a second input end of said first NAND gate, an output end of said first NAND coupled to an input end of said second passgate;

an output end of said third passgate coupled to an input end of said fourth inverter and to an output end of said fourth passgate;

an output end of said fourth inverter coupled to an input end of said fifth inverter and to an input end of said sixth inverter;

an output end of said fifth inverter coupled to an input end of said fourth passgate;

an output end of said sixth inverter coupled to said output of said resetable control circuit.

12. (Original) The device of claim 11, further comprising:

a reset signal generator, containing a NAND gate, a first input of said NAND gate, a second input of said NAND gate, an output of said NAND gate;

said first input coupled to an OUT end of said sense amplifier, said second input coupled to an OUTB end of said sense amplifier, and said output coupled to said third input of said resetable control circuit.

13. (Currently Amended) A device to control a sense amplifier, comprising:

a flip flop ~~control~~ circuit containing a first input, a second input, a third input, and an output; said first input coupled to said output ~~or to a ground~~; said second input coupled to receive a start signal; said third input coupled to receive output signals of said sense amplifier; and said output coupled to said sense amplifier;

wherein said flip-flop circuit is a D flip-flop circuit and said first input is a data signal for said D flip-flop circuit.

14. (Previously Presented) The device of claim 13 wherein said first input, said second input, said third input, and said output are initially low; when said second input

goes high and then goes low again, said output goes high; when said third input goes high, said output goes low.

15. (Previously Presented) The device of claim 13 further comprising:

a reset signal generator, containing a first input coupled to an OUT end of said sense amplifier, a second input coupled to an OUTB end of said sense amplifier, and an output coupled to said third input of said resetable control circuit; and

when either OUT or OUTB reaches a predetermined low voltage level, said output of said reset signal generator goes high.

16. (Previously Presented) The device of claim 13 wherein said start signal is a triggered clock for said D flip-flop circuit.

17. (Previously Presented) The device of claim 13 wherein said start signal is a pseudo word line signal.

18. (Previously Presented) The device of claim 13 wherein said third input is a reset signal for said D flip-flop circuit.

19. (Previously Presented) The device of claim 13 wherein said first input being a data signal for said D flip-flop, said second input being a triggered clock for said D flip-flop, said third input being a reset signal for said D flip-flop, and said output are initially low; when said triggered clock goes high and then goes low again, said output goes high; when said reset signal goes high, said output goes low.

20. (Previously Presented) The device of claim 13 wherein said flip flop circuit further comprises a first passgate, a second passgate, a third passgate, and fourth passgate; a first

inverter, a second inverter, a third inverter, a fourth inverter, a fifth inverter, and a sixth inverter; and a first NAND gate;

said first input of said circuit coupled to an input end of said first passgate, an output end of said first passgate is coupled to an output end of said second passgate and an input end of said third inverter;

said second input of said circuit coupled to an input end of said first inverter; a C end of said first passgate, a CB end of said second passgate, a CB end of said third passgate, and a C end of said fourth passgate;

said third input of said circuit coupled to an input end of said second inverter;

an output end of said first inverter coupled to a CB end of said first passgate, a C end of said second passgate, a C end of said third passgate, and a CB end of said fourth passgate;

an output end of said third inverter coupled to a first input end of said first NAND gate and to an input end of said third passgate;

an output end of said second inverter coupled to a second input end of said first NAND gate, an output end of said first NAND gate coupled to an input end of said second passgate;

an output end of said third passgate coupled to an input end of said fourth inverter and to an output end of said fourth passgate;

an output end of said fourth inverter coupled to an input end of said fifth inverter and to an input end of said sixth inverter;

an output end of said fifth inverter coupled to an input end of said fourth passgate;

an output end of said sixth inverter coupled to said output of said resetable control circuit.

21. (Previously Presented) The device of claim 20, further comprising:

a reset signal generator, containing a NAND gate, a first input of said NAND gate, a second input of said NAND gate, an output of said NAND gate;

said first input coupled to an OUT end of said sense amplifier, said second input coupled to an OUTB end of said sense amplifier, and said output coupled to said third input of said resetable control circuit.

22. (Previously Presented) A device to control a sense amplifier, comprising:

a D flip flop circuit containing a first input, a second input, a third input, and an output; said first input coupled to said output or to a ground; said second input coupled to receive a start signal; said third input coupled to receive output signals of said sense amplifier; and said output coupled to said sense amplifier;

a first passgate, a second passgate, a third passgate, and fourth passgate; a first inverter, a second inverter, a third inverter, a fourth inverter, a fifth inverter, and a sixth inverter; and a first NAND gate;

said first input of said circuit coupled to an input end of said first passgate, an output end of said first passgate coupled to an output end of said second passgate and an input end of said third inverter;

said second input of said circuit coupled to an input end of said first inverter; a C end of said first passgate, a CB end of said second passgate, a CB end of said third passgate, and a C end of said fourth passgate;

said third input of said circuit coupled to an input end of said second inverter;

an output end of said first inverter coupled to a CB end of said first passgate, a C end of said second passgate, a C end of said third passgate, and a CB end of said fourth passgate;

an output end of said third inverter coupled to a first input end of said first NAND gate and to an input end of said third passgate;

an output end of said second inverter coupled to a second input end of said first NAND gate, an output end of said first NAND coupled to an input end of said second passgate;

an output end of said third passgate coupled to an input end of said fourth inverter and to an output end of said fourth passgate;

an output end of said fourth inverter coupled to an input end of said fifth inverter and to an input end of said sixth inverter;

an output end of said fifth inverter coupled to an input end of said fourth passgate;

an output end of said sixth inverter coupled to said output of said resetable control circuit.

23. (Previously Presented) The device of claim 22, further comprising:

a reset signal generator, containing a NAND gate, a first input of said NAND gate, a second input of said NAND gate, an output of said NAND gate;

said first input coupled to an OUT end of said sense amplifier, said second input coupled to an OUTB end of said sense amplifier, and said output coupled to said third input of said resetable control circuit.